intel

8020H

PRELIMINARY

HMOS SINGLE-COMPONENT 8-BIT MICROCOMPUTER

- 8-bit CPU, ROM, RAM, I/O in Single 20-pin Package
- Single +5V Supply (+4.5V to 6.5V)
- 8.38 μsec Cycle with 3.58 MHz XTAL. All Instructions 1 or 2 cycles.
- Instructions—8048 Subset
- 1K x 8 ROM
  64 x 8 RAM
  13 I/O Lines
- Internal Timer/Counter
- 30mA Operation @ 25° C

The Intel® 8020H is a cost-effective single-chip microcomputer for high volume, cost-sensitive applications such as home entertainment products, appliances and simple control jobs. The 8020H is an 8-bit computer fabricated on a single silicon chip using Intel's advanced N-channel silicon gate HMOS process.

The 8020H key features include a subset of the industry standard 8048's instruction set optimized for the consumer an appliance marketplaces. Some of these features are a 1K × 8 program memory, a 64 × 8 data memory, 13 I/O lines and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. The 20-pin package provides board real estate savings.

A specific requirement in many of these market-type applications is the need for more I/O. The 8020H has instructions and hardware on-board to interface to TTL I/O expansion packages.

To make efficient use of the program memory size, the 8020H has an instruction set optimized for byte efficiency and control. No instructions are longer than 2 bytes, with 70% of the instructions at 1 byte. For control-oriented applications, arithmetic instructions are supported using binary and BCD operands.

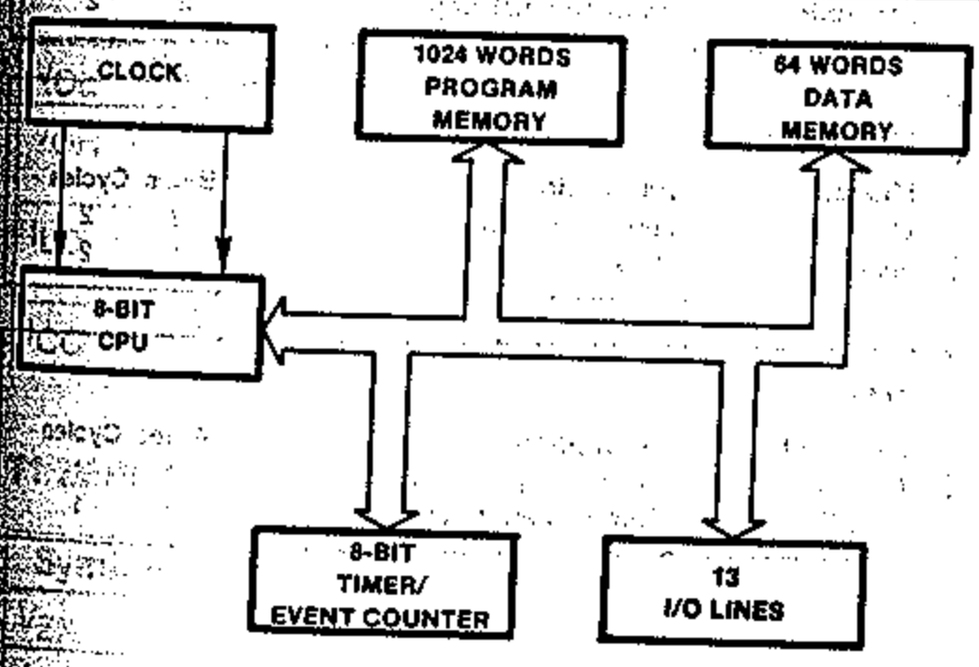

Figure 1. Block Diagram

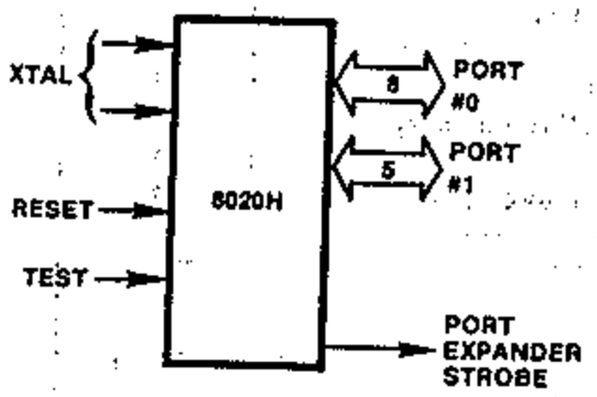

Figure 2. Logic Symbol

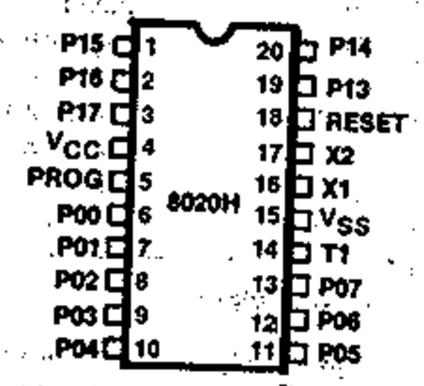

Figure 3. Pin Configuration

Table 1. Pin Description

Symbol	Pin No.	Function
V_{SS}	15	Circuit GND potential
V_{CC}	4	+5V power supply
PROG	5	Output strobe for TTL I/O expansion
P00–P07 Port 0	6–13	8-bit quasi-bidirectional port
P3–P17 Port 1	19–20 1–3	5-bit quasi-bidirectional port
T1	14	Input pin testable using the JT1 and JNT1 instructions. Can be designated the timer/event counter input using the STRT CNT instruction. Also allows zero-crossover sensing of slowly moving AC inputs
RESET	18	Input used to initialize the processor by clearing status flip-flops and setting program counters to zero.
XTAL1	16	One side of crystal or inductor input for internal oscillator. Also input for external source. (Not TTL compatible.)
XTAL2	17	Other side of timing control element.

Table 2. Instruction Set

Accumulator

Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, # data	Add immediate to A	2	2
ADDC A, R	Add with carry	1	1
ADDC A, @R	Add with carry	1	1
ADDC A, # data	Add with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, # data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A, @R	Or data memory to A	1	1
ORL A, # data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL A, # data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal Adjust A	1	1
SWAP A	Swap nibles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Input/Output

Mnemonic	Description	Bytes	Cycles
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2

Registers

Mnemonic	Description	Bytes	Cycles
INC R	Increment register	1	1
INC @R	Increment data memory	1	1

Branch

Mnemonic	Description	Bytes	Cycles
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and Jump on R not zero	2	2
JC addr	Jump on Carry = 1	2	2
JNC addr	Jump on Carry = 0	2	2
JZ addr	Jump on A Zero	2	2
JNZ addr	Jump on A not Zero	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JTF addr	Jump on timer flag	2	2

Subroutine

Mnemonic	Description	Bytes	Cycles
CALL	Jump to subroutine	2	2
RET	Return	1	2

Flags

Mnemonics	Description	Bytes	Cycles
CLR C	Clear Carry	1	1
CPL C	Complement Carry	1	1

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Table 2. Instruction Set Summary (cont.)

Data Moves

Mnemonics	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, # data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, # data	Move immediate to register	2	2
MOV @R, # data	Move immediate to data memory	2	2
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and register	1	1
MOVP A, @A	Move to A from current page	1	2

Timer/Counter

Mnemonic	Description	Bytes	Cycles
MOV A, T	Read Timer/Counter	1	1
MOV T, A	Load Timer/Counter	1	1
STRT T	Start Timer	1	1
STRT CNT	Start Counter	1	1
STOP TCNT	Stop Timer/Counter	1	1

Mnemonics	Description	Bytes	Cycles
NOP	No Operation	1	1

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0° C to 70° C
Storage Temperature ..... −65° C to +150° C
Voltage on Any Pin with Respect to Ground ..... −0.5V to +7V
Power Dissipation 1W

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0° C to 70° C, V_{CC} = 5.5V ± 1V, V_{SS} = 0V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage (All except XTAL 1 & 2, T1, RESET)	3.0		V_{CC}	V	
V_{IH1}	Input High Voltage (XTAL 1 & 2, T1, RESET)	3.8		V_{CC}	V	
$V_{IH(10\%)}$	Input High Voltage (All except XTAL 1 & 2, T1, RESET)	2.0		V_{CC}	V	V_{CC} = 5.0V ± 10%
$V_{IH1(10\%)}$	Input High Voltage (XTAL 1 & 2, T1, RESET)	3.5		V_{CC}	V	V_{CC} = 5.0V ± 10%
V_{OL}	Output Low Voltage			0.45	V	I_{OL} + 1.6 mA
V_{OH}	Output High Voltage (All unless Open Drain)	2.4			V	I_{OH} = 40 μA
I_{LO}	Output Leakage Current (Open Drain Option—Port 0)			±10	μA	V_{SS} + 0.45 ≤ V_{IN} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		30	60	mA	

ZERO CROSS CHARACTERISTICS (T_A = 0° C to 70° C, V_{CC} = 5.5V ± 1V, V_{SS} = 0V, C_L = 80 pF)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{ZX}	Zero-Cross Detection Input (T1)	1	3	V_{PP}	AC Coupled, C = .2μF
A_{ZX}	Zero-Cross Accuracy		±135	mV	60 Hz Sine Wave
f_{ZX}	Zero-Cross Detection Input Frequency (T1)	0.05	1	kHz	
t_{CY}	Cycle Time	8.38	50.0		3.58 MHz XTAL = 8.38 μs t_{CY}

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8020H FUNCTIONAL SPECIFICATIONS

The following is a functional description of the major elements of the 8020H.

Program Memory

The 8020H contains 1K x 8 of mask programmable ROM. No external ROM expansion capability is provided.

Data Memory

A 64 x 8 dynamic RAM is located on chip for data storage. All locations are indirectly addressable and eight designated locations are directly addressable. Also, included in the memory is the address stack, addressed by a 3-bit stack pointer.

Memory is organized as shown in Figure 4. The least significant 8 addresses, 0–7, are directly addressable by any of the 11 direct register instructions. The locations are readily accessible for a variety of operations with the least number of instruction bytes required for their manipulation.

Registers 0 and 1 have another function, in that they can be used to indirectly address all locations in memory, using the indirect register instructions. These indirect RAM address registers, IRAR's, are especially useful for repetitive-type operations on adjacent memory locations. The indirect register instruction specifies which IRAR to use, and the contents of the IRAR is used to address a location in RAM. The contents of the addressed location is used during the execution of the instruction and may be modified. A value larger than 63 should not be preset in the IRAR when selected by an indirect register instruction. IRAR's may point to addresses 0–7, if desired.

Locations 8–23 may be used as the address stack. The address stack enables the processor to keep track of the return addresses generated from CALL instructions. A 3-bit stack pointer (SP) supplies the address of the locations to be loaded with the next return address generated. The SP to this pushdown stack is incremented by one after a return address is stored, and decremented by one before an address is fetched during a RET. The unincremented program counter address is stored in the address stack. The stack contents is incremented before being loaded into the program counter during a return from subroutine. A total of 8 levels of nesting is possible. The SP is initialized to location 8 upon RESET. Since each address is 10-bits long, two bytes must be used to store a single address. The SP is incremented and decremented by one, but each increment or decrement moves the address pointed to by two. Therefore, only even numbered addreses are pointed to.

If a particular application does not require 8 levels of nesting, the unused portion of the stack may be used as any other indirectly addressable stratchpad location. For example, if only 3 levels of subroutine nesting are used, then only locations 8–13 need be reserved for the address stack, and locations 14–63 can be used for data storage.

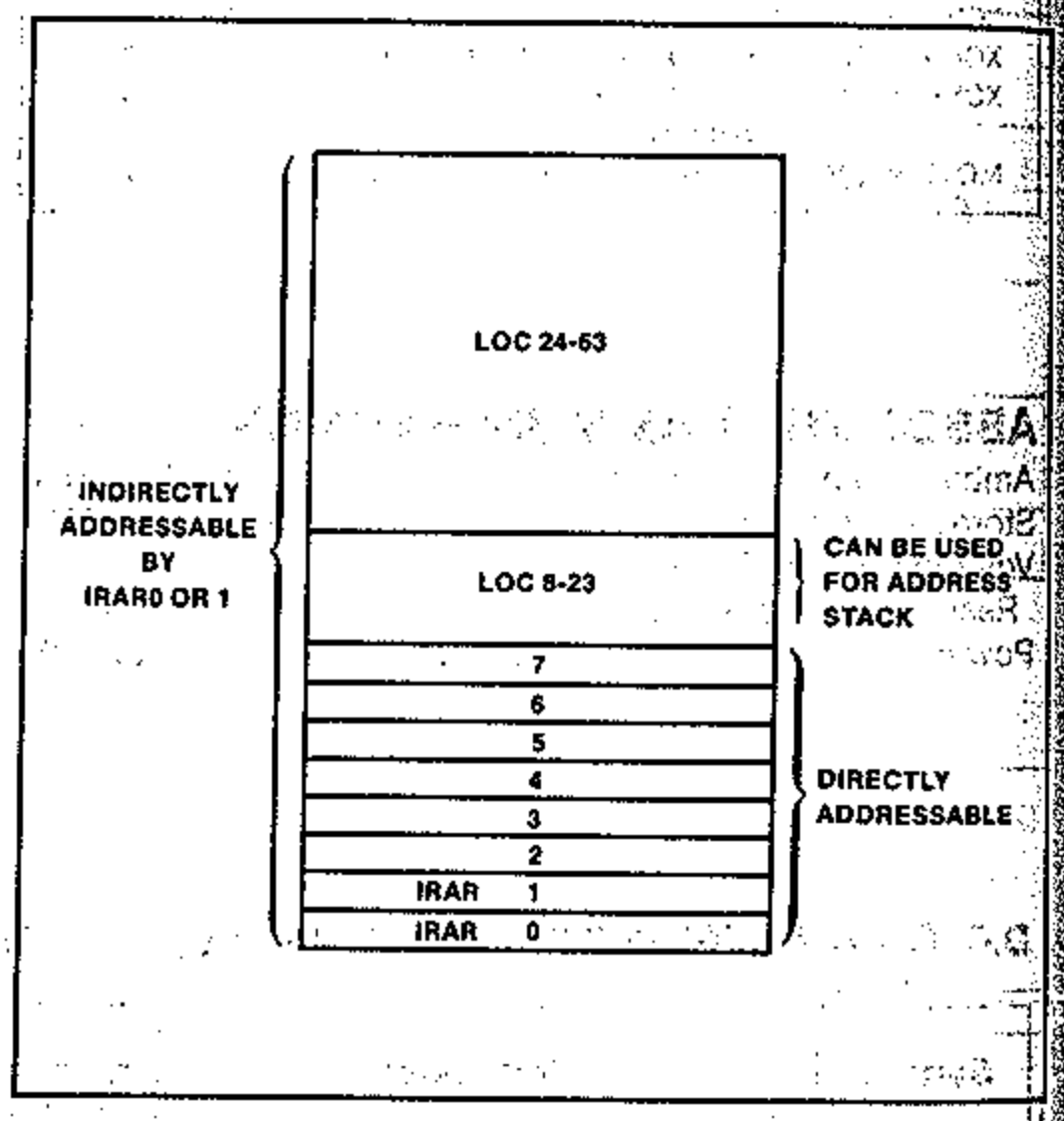

Figure 4. Internal RAM Organization.

Oscillator and Clock

The 8020H contains its own onboard oscillator and clock circuit, requiring only an external timing control element. This control element can be a crystal, inductor, or clock in. The capacitor normally required in inductor timing control operation is integrated onto the 8020H. All internal time slots are derived from the external element, and all outputs are a function of the oscillator frequency. Pins XTAL1 and XTAL2 are used to input the particular control element. An instruction cycle consists of 10 states, and each state is a time slot of 3 oscillator periods. (See Figure 5.) Therefore, to obtain a 10 μsec instruction cycle, a 3 MHz crystal should be used. An oscillator frequency of approximately 3 MHz may also be obtained by connecting a 470 μH inductor between XTAL1 and XTAL2. Note that the required inductance may vary and should be adjusted as necessary.

The 8020H utilizes dynamic RAM and certain other dynamic logic. Due to the clocking required with dynamic circuits, the oscillator frequency must be equal to or greater than 600K Hz, or improper operation may occur.

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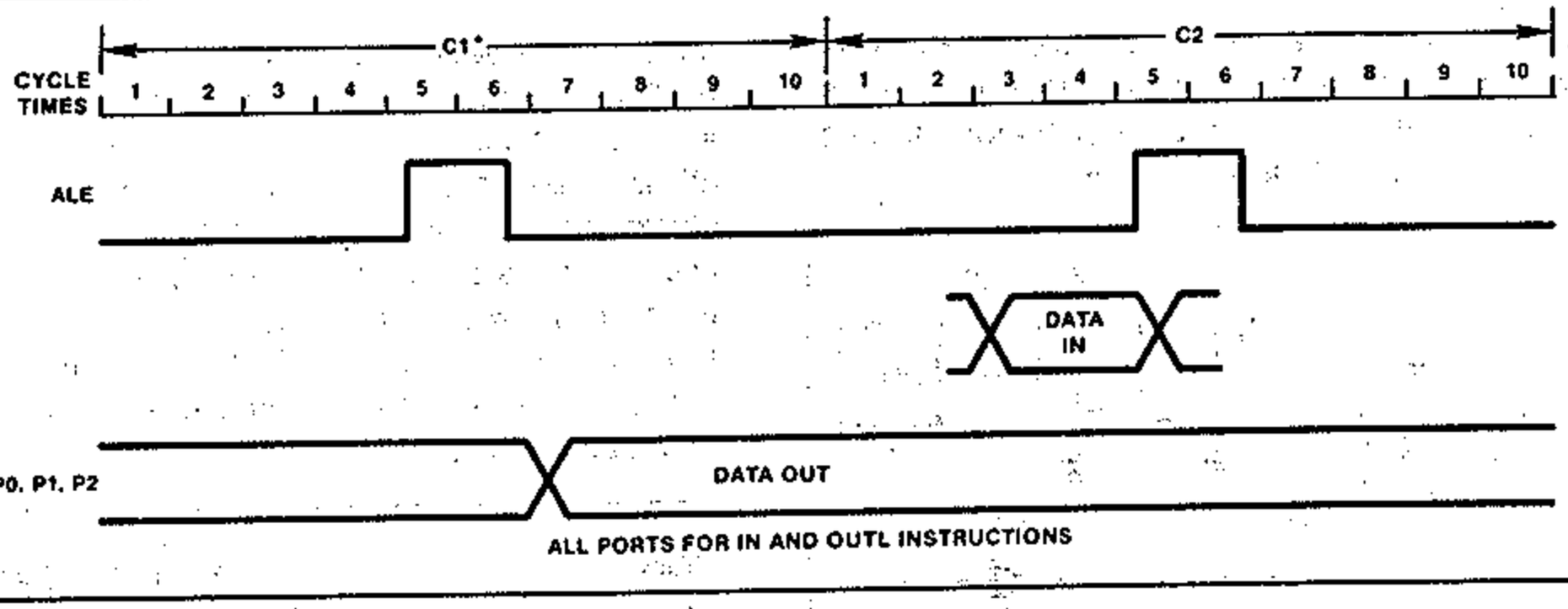

Figure 5. 8020H Timing Diagram

Timer/Event Counter

The 8020H has internal timer/event counter circuits that can monitor elapsed time or count external events that occur during program execution. The circuit has an 8-bit binary up-counter that is presettable and readable with two MOV instructions. These instructions transfer the contents of the accumulator to the counter and vice versa. The counter content is not affected by Reset, and is initialized solely by the MOV T,A instruction. The counter is stopped by a RESET or STOP TCNT instruction and remains stopped until started as a timer by a STRT T instruction or as an event counter by a STRT CNT instruction. Once started, the counter increments to its maximum count (FF), and overflows to zero. The count continues until stopped by a STOP TCNT instruction or RESET. The increment from maximum count to zero (overflow) sets an overflow flag. The state of the overflow flag is testable with the conditional jump instruction JTF. The flag is reset by JTF but not by executing a RESET, unlike the 8748.

By a MOV T,A instruction, the contents of the accumulator are loaded to the timer. At the STRT T command an internal prescaler is zeroed and thereafter increments once each 30 input clocks (once each single cycle instruction, twice each double cycle instruction). The prescaler is a divide by 32. At the (11111) to (00000) transition the timer is incremented. The timer is 8-bits and an overflow (FFH) to (00H) timer flag is set. A conditional branch instruction (JTF) is available for testing this flag, the flag being reset each test. Total count capacity for the timer is $2^8 \times 2^5 = 8192$ or 81.9 msec at a 10 μsec cycle time. Contents of the timer are moved to the accumulator by the MOV A,T instruction without disturbing the counting process. The timer stops upon the STOP TCNT instruction.

The STRT CNT instruction connects the T1 input pin to the event counter input and enables the counter. Subsequent high-to-low transitions on T1 increment the counter. The maximum rate at which the counter can increment is once per three instruction cycles (30μs for a 3 MHz oscillator). There is no minimum frequency. T1 input must remain high for at least 500ns after each transition. The event counter is stopped by a STOP TCNT instruction.

Input/Output Capabilities

The 8020H I/O configurations are highly flexible. A number of different configurations are possible, tailoring an 8020H to a given task. Other than the power supply and dedicated pins, all other pins (13) can be used for input, output, or both, depending on the configuration.

All ports are quasi-bidirectional to facilitate standalone use. A simplified schematic of the quasi-bidirectional interface is shown in Figure 6. This configuration allows buffered outputs, and also allows external input. Data written to these ports is statically latched and remains unchanged until rewritten. As input ports these lines are non-latching, i.e., inputs must be present until read by an input instruction. When writing a "0" or low value to these ports, the large pulldown device sinks an external TTL load. When writing a "1", a large current is supplied through the large pullup device to allow a fast data transfer. After a short time (less than one instruction cycle), the large device is shut off and the small pullup maintains the "1" level indefinitely. However, in this situation, an input device capable of overriding the small amount of sustaining current supplied by the pullup device can be read. (Alternatively, the data written can be read.) So, by writing a "1" to any particular pin, that pin can serve either as a true high-level latched output pin, or as just a pullup resistor on an input. This allows maximum user flexibility in selecting his input or latched output pins, with a minimum of external components.

Port 00-07 is also quasi-bidirectional, except there is no large pullup device. As outputs, this port is essentially open drain.

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By mask option the small pullup devices on P00–P07 may be deleted on any pin providing a true open drain output. This is useful in driving analog circuits and certain loads, such as keyboards.

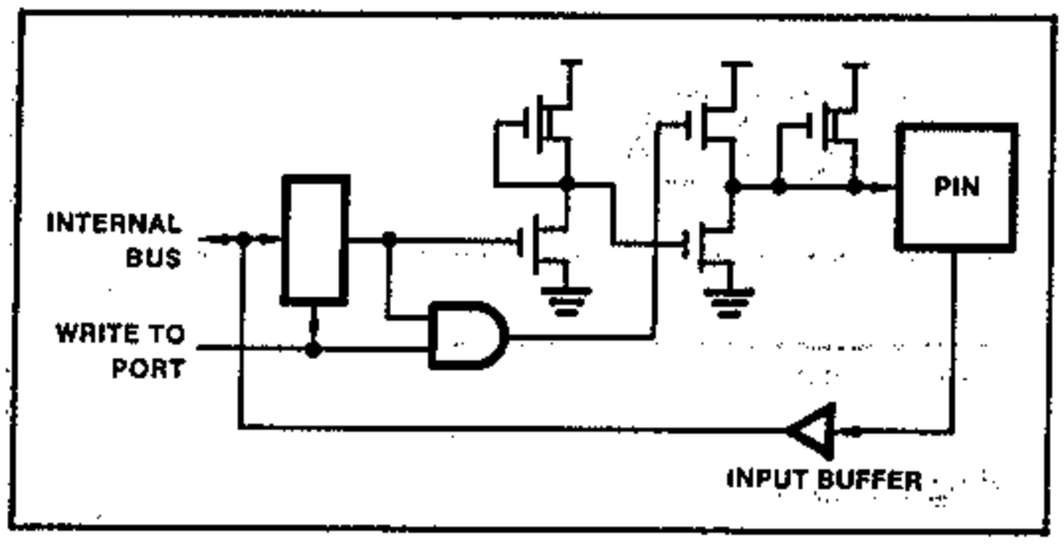

Figure 6. Quasi-Bidirectional Port Structure

T1 Input

The 8020H T1 input line can be used as an input for the following functions:

- Event Counter (external input)
- Test input for branch instructions
- Zero voltage crossing detection

The operation of T1 as an input to the Event Counter is described in the Timer/Event Counter section. When used as a test input, the JT1 and JNT1 instructions test for 1 and 0 levels, respectively.

The T1 pin can also be used to detect the zero crossing of slowly moving AC signals (60 Hz). The self-biasing circuit shown in Figure 7 permits the Test 1 input to detect when the input voltage crosses zero within ±5%; the voltage is then coupled through a 1.0μf capacitor. Maximum input voltage is 3V peak-to-peak. The zero cross detection is especially useful in SCR control of 60 Hz power and in developing time-of-day and other timing routines. As a ROM mask option there is a pullup resistor that is useful for switch contact input or standard TTL.

The 8020H can use standard low cost TTL to expand the number of I/O lines.

CPU

The 8020H CPU has arithmetic and logical capability. A wide variety of arithmetic and logic instructions may be exercised, which affect the contents of the accumulator, and/or direct or indirect scratchpad locations. Provisions have been made for simplified BCD arithmetic capability using the DAA, SWAP A and XCHD instructions. In addition, MOVP A,@A allows table lookup for display formating and constants. The conditional branch logic within the processor enables several conditions internal and external to the processor to be tested by the users program. Use the conditional jump instructions with the tests listed below to effect a change in the program execution sequence:

Test	Jump Condition	Jump Instructions
Accumulator	A=0 A≠0	JZ JNZ
Carry Flag	0 1	, JC
Timer Overflow Flag	— 1	JTF
Test Input-T1	0 1	JNT1, JT1

Reset

A positive-going signal to the RESET input resets the necessary miscellaneous flip-flops and sets the program counter and stack pointer to zero.

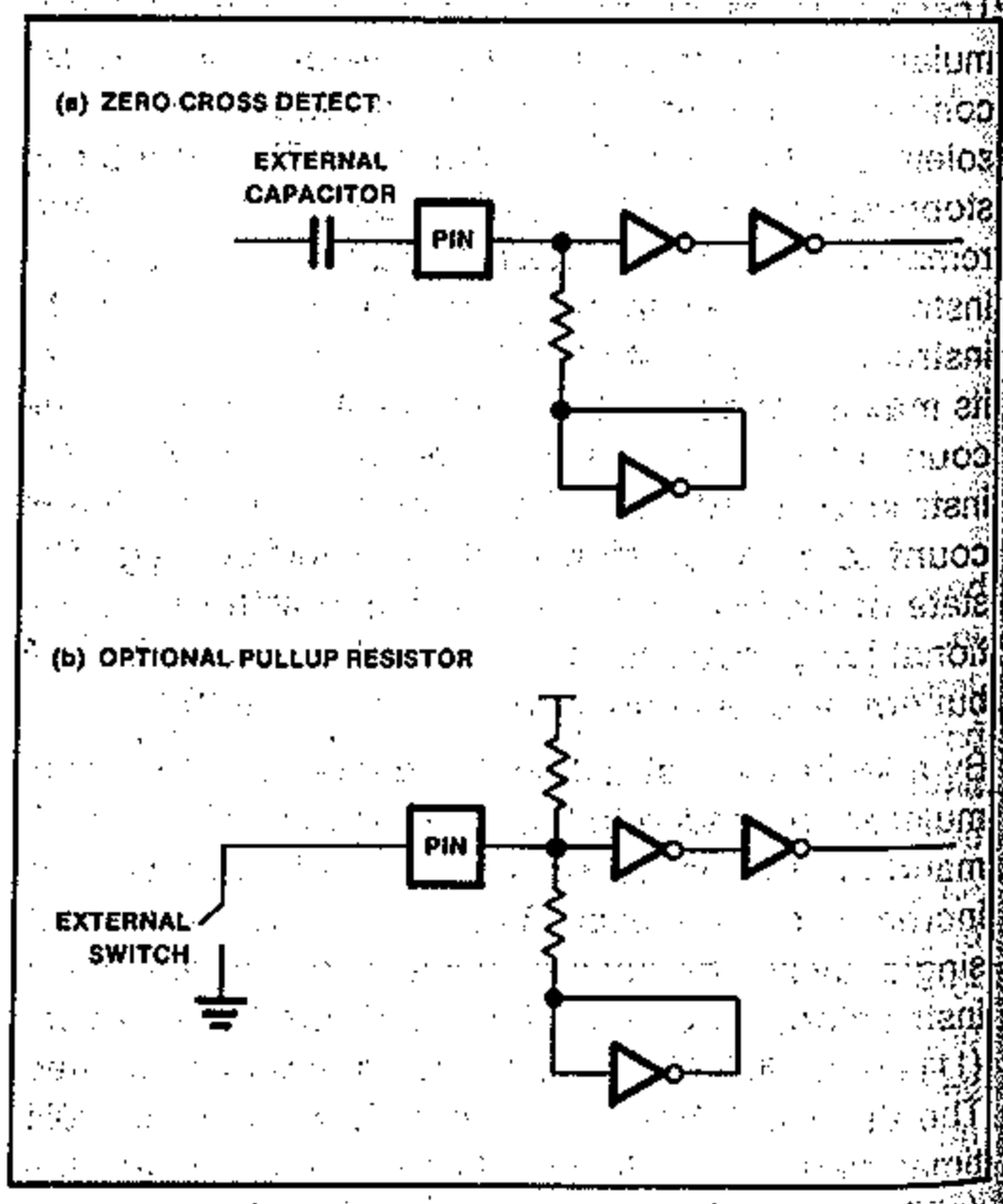

Figure 7. Test 1 Pin

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